WHAT IS CLAIMED IS:

1. A method of developing an ASIC, comprising:

developing hardware and software concurrently; and

co-simulating the hardware and software therebetween via a network while the hardware and software are being developed.

2. The method of claim 1, wherein the hardware is developed on a workstation.

3. The method of claim 1, wherein the software is developed on a target board.

4. The method of claim 1, wherein the network is an TCP/IP protocol.

5. The method of claim 1, wherein the hardware to be co-simulated is described by a high-level language model.

6. The method of claim 1, further comprising receiving test inputs for the co-simulation from a real working environment.

7. The method of claim 1, further comprising receiving test inputs for the co-simulation from a test tool.

8. A method of co-simulating hardware and software in ASIC development, comprising:

requesting an access to a hardware model from a hardware side to a software side via a network;

invoking a function call by a CPU server at a software side;

sending an access request from the hardware side to the CPU server at the software side via the network; and

routing the access request to the hardware model.

9. The method of claim 8, wherein the function call is a READ function call.

10. The method of claim 8, wherein the function call is a WRITE function call.

11. The method of claim 8, further comprising requesting a hardware model interrupt, and a function call to handle the interrupt being invoked by the software via the network.

12. An apparatus for hardware and software co-simulation in ASIC development comprising:

a hardware model to represent a hardware board circuit to be co-simulated/tested, the hardware model being developed on a workstation;

a software to command and control accesses of the hardware model, the software being developed/debugged on a target board concurrently with a design of the hardware model; and

a network, coupled between the workstation and the target board, to communicate a command from the software to the hardware model and to route contents of the command between the workstation and the target board.

13. The apparatus of claim 12, wherein the hardware model comprises a CPU bus functional model which communicates the hardware model to a CPU server of the target board via the network.

14. The apparatus of claim 13, wherein the software is loaded on the CPU server.

15. The apparatus of claim 12, wherein the network is an TCP/IP protocol.

16. The apparatus of claim 12, wherein the hardware model is capable of receiving test inputs for co-simulation from a real working environment.

17. The apparatus of claim 12, wherein the hardware model is capable of receiving test inputs for co-simulation from a test tool.